

IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.- 10. (Cancelled)

11. (New) A semiconductor memory element, comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate

a channel region formed in said semiconductor substrate between said source region and said drain region;

a silicon oxide film arranged on a portion of said semiconductor substrate corresponding to said channel region, wherein a plurality of silicon microcrystal grains are formed in said silicon oxide film; and

a gate electrode formed over said silicon oxide film and comprised of a metal or a semiconductor to control electric potential of said channel region,

wherein a perimeter of each of said silicon microcrystal grains is covered with said silicon oxide film so that each of said microcrystal grains constitutes an independent and isolated charge storage region such that said plurality of said charge storage regions are electrically disconnected.

12. (New) A semiconductor memory element according to claim 11,

wherein an electric potential to be applied to said gate electrode upon writing of data and an electric potential to be applied to said gate electrode upon erasing of data have the same polarity.

13. (New) A semiconductor memory element according to claim 11,
wherein said plurality of microcrystal grains have a mean size of
approximately 10 nm.

14. (New) A semiconductor memory element according to claim 12,
wherein said plurality of microcrystal grains have a mean size of
approximately 10 nm.

15. (New) A semiconductor memory element according to claim 11,
wherein said plurality of charge storage regions store charges from the same
bit of data.

16. (New) A semiconductor memory element according to claim 12,
wherein said plurality of charge storage regions store charges from the same
bit of data.

17. (New) A semiconductor memory element, comprising:
a source region formed in a semiconductor substrate;
a drain⁰³⁴ formed in said semiconductor substrate;
a channel formed in said semiconductor substrate between said source region
and said drain region;
a silicon oxide film arranged on a portion of said semiconductor substrate
corresponding to said channel region; and
a gate electrode formed over said silicon oxide film and comprised of a metal
or semiconductor to control electrical potential of said channel region,

wherein said silicon oxide film includes means for dispersing charges corresponding to one bit of data written into said semiconductor element into a plurality of independent isolated charge storage regions.

18. (New) A semiconductor memory element according to claim 17,

wherein said means for dispersing charges includes a plurality of silicon microcrystal grains formed in said silicon oxide film which are electrically disconnected from one another.

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19. (New) A semiconductor memory element according to claim 18,

wherein said plurality of microcrystal grains have a mean size of approximately 10 nm.

20. (New) A semiconductor memory element according to claim 17,

wherein an electric potential to be applied to said gate electrode upon writing of data and an electric potential to be applied to said gate electrode upon erasing of data have the same polarity.
